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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,815	02/03/2004	Byung Hyun An	3449-0302P	9530

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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
10/31/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/769,815	AN, BYUNG HYUN	
	Examiner	Art Unit	
	Jean E. Lesperance	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *August 9, 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-11,15-17 and 20-25* is/are rejected.

7)☒ Claim(s) *12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/17/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed August 9, 2007 is entered and claims 1-17 and 20-25 are pending.

2. The indicated allowability of claims 1-17 and 20-25 is withdrawn in view of the newly discovered reference(s) to Kim (6069610) and Tati et al. (6011880). Rejections based on the newly cited reference(s) follow.

Response to Arguments

3. Applicant's arguments with respect to claims 1-17 and 20-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 15, 17, and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6069619 ("Kim") in view USPN 6011880 ("Tani et al").

Regarding claim 1, Kim teaches the microcomputer 22 stores a current DPMS state in response to the detection of horizontal and vertical sync signals received via the D-sub input port 21 as well the proper connection of the signal cable 30 (column 3, lines 45-48); based on the stored DPMS status information, the microcomputer 22 determines the proper DPMS mode and sets a DPMS control output via a DPMS output port, accordingly (column 3, lines 53-55); A microcomputer 22 comprises an internal

memory (not shown), such as an EEPROM, which stores information regarding the status of the display device 20 (column 3, lines 42-44). The prior art teach all the claimed limitations with the exception of providing a comparator.

However, Tani et al. teach a comparator Fig.3 (10).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the comparator as taught by Tani et al. in the display apparatus disclosed by Kim because this would provide an encoded symbol reader that can accurately decode a two-dimensional symbol.

Regarding claim 2, it is rejected on the same basis as claim 1.

Regarding claim 3, Kim teaches the microcomputer 22 interprets an activation of any one of user keys 26, which are normally conventional display controls located on the front panel of the display device, as a program interrupt signal (column 3, lines 58-61).

Regarding claim 4, Kim once a user key input (interrupt) is detected, the microcomputer 22 generates, using internal oscillators (not shown), horizontal and vertical synchronous signals in step S43 (column 4, lines 48-51).

Regarding claims 5 and 6, Tani et al. teach the image signal (analog) output by CCD 43 is amplified by an amplifier 8 and fed to the A/D converter 9 where it is converted into an 8 bit digital image signal (having 256 steps of gradation). The amplified image signal (analog) Is also transmitted to the terminal 21 (column 5, lines 33-37).

Regarding claim 7, Kim A microcomputer 22 comprises an internal memory (not shown), such as an EEPROM, which stores information regarding the status of the display device 20 (column 3, lines 42-44).

Regarding claim 8, Tani et al. teach the 8 bit digital image signal is transmitted from the A/D converter 9 to a comparator 10. At the same time, threshold data is transmitted to the comparator 10 from the memory 13 via data bus 17 and the CPU 15. The 8 bit digital image signal is compared with the threshold data (also an 8 bit digital signal) and 1 bit digital data is generated (column 5, lines 38-43).

Regarding claim 9, Kim teaches a microcomputer, being connected to the input port and comprising an internal memory, for generating horizontal and vertical synchronous signals in response to the horizontal and vertical sync signals received by the input port; at least one user key, mounted on the display device, for inputting a key signal to the microcomputer (column 2, lines 56-62).

Regarding claims 10 and 11, Tani et al. teach the memory 27 also stores a reference threshold data. When the test mode is selected, the reference image data and the reference test data are transmitted to the comparator 10 and the 1-bit binary data is generated. In the test mode, the comparator 10 outputs a 1-bit binary data based on the reference image data and the reference threshold data (See figure 8).

Regarding claim 15, Kim teaches the microcomputer 22 stores a current DPMS state in response to the detection of horizontal and vertical sync signals received via the D-sub input port 21 as well the proper connection of the signal cable 30 (column 3, lines 45-48); based on the stored DPMS status information, the microcomputer 22

determines the proper DPMS mode and sets a DPMS control output via a DPMS output port, accordingly (column 3, lines 53-55); A microcomputer 22 comprises an internal memory (not shown), such as an EEPROM, which stores information regarding the status of the display device 20 (column 3, lines 42-44); data processed by a CPU 11 of a main body 10 of a personal computer system is converted to an RGB video signal by a video card 12 (column 3, lines 28-30). The prior art teach all the claimed limitations with the exception of providing a comparator and an A/D converter.

However, Tani et al. teach a comparator (10) and an A/D converter (9) (see Fig.3). (10).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the comparator and an A/D converter as taught by Tani et al. in the display apparatus disclosed by Kim because this would provide an encoded symbol reader that can accurately decode a two-dimensional symbol.

Regarding claim 17, Kim teaches the microcomputer 22 stores a current DPMS state in response to the detection of horizontal and vertical sync signals received via the D-sub input port 21 as well the proper connection of the signal cable 30 (column 3, lines 45-48) wherein the microcomputer functions as a comparator.

Regarding claim 20, Kim teaches the microcomputer 22 stores a current DPMS state in response to the detection of horizontal and vertical sync signals received via the D-sub input port 21 as well the proper connection of the signal cable 30. This hardware connection is determined using, for example, a pull-up resistor to apply a logic "high" voltage signal whenever there is no ground signal provided from the video card 12 via

the signal cable 30 having a cable detection line (column 3, lines 45-48). The prior art teaches all the claimed limitations with the exception of providing a storage command signal. However, Tani et al. teach the CPU 15 can transmit an instruction to start writing/reading to the memory controller 14 synchronously with the horizontal/vertical synchronous signals (see Figure 3).

Thus, it would have been obvious to a person ordinary skill in the art at the time the invention was made to utilize the instruction as taught by Tani et al. in the processing display apparatus disclosed by Kim because this would provide an encoded symbol reader that can accurately decode a two-dimensional symbol.

Regarding claim 21, it is rejected on the same basis as claim 20.

Regarding claim 22, Kim teaches the microcomputer 22 stores a current DPMS state in response to the detection of horizontal and vertical sync signals received via the D-sub input port 21 as well the proper connection of the signal cable 30. This hardware connection is determined using, for example, a pull-up resistor to apply a logic "high" voltage signal whenever there is no ground signal provided from the video card 12 via the signal cable 30 having a cable detection line (column 3, lines 45-48); the microcomputer 22 reads the stored status data corresponding to the current DPMS mode in step S45, and then transmits a corresponding OSD drive signal to the OSD circuit 23 through an OSD drive output port in step S46 (column 4, lines 54-57); the horizontal and vertical deflection circuit 25 receives the horizontal and vertical synchronous signals generated in the microcomputer 22 and thus synchronizes the OSD video signal by outputting a sawtooth wave to the deflection yoke in response to

these "artificial" sync signals (column 4, lines 62-67). The prior art teaches all the claimed limitations with the exception of providing a storage command signal. However, Tani et al. teach the CPU 15 can transmit an instruction to start writing/reading to the memory controller 14 synchronously with the horizontal/vertical synchronous signals (see Figure 3).

Thus, it would have been obvious to a person ordinary skill in the art at the time the invention was made to utilize the instruction as taught by Tani et al. in the processing display apparatus disclosed by Kim because this would provide an encoded symbol reader that can accurately decode a two-dimensional symbol.

Regarding claim 23-25, they are rejected on the same basis as claim 20 (see Figures 1 and 2 of Kim and Figure 3 of Tani et al.).

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6069619 ("Kim") in view USPN 6011880 ("Tani et al") and further in view of USPN 6658583 (Kudo et al).

Regarding claim 16, the combination of Kim and Tani et al. fails to teach a clock generator, connected to the A/D converter and scaler, for signal synchronization or turning.

However, Kudo et al. teach the microcomputer comprises a CPU for executing instructions (in a broad sense, processor), a ROM 302, a RAM 304, a clock generator 306, a pre-scaler 308, a programmable timer 310, a reset circuit 314, a DMA controller 316, an interrupt controller 318, a bus controller 320, an A/D converter 322, an input port 324, an output port 326, an I/O port 328 and so on (see Figure 8).

Thus, it would have been obvious to a person ordinary skill in the art at the time the invention was made to utilize the clock generator as taught by Kudo et al. in the combination disclosed by Kim and Tani et al. because this would provide a PWM control circuit, microcomputer and electronic equipment which can generate a high-resolution PWM signal through a reduced circuit scale.

Allowable Subject Matter

6. Claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: the claimed invention is directed to a processing display data.

Dependent claim 12 identifies a uniquely distinct feature "wherein the Micom is arranged to save the image signal in the memory in response to a first command signal outputted from the comparator, and end storage of the image signal in response to a second command signal outputted from the comparator".

Dependent claim 13 identifies a uniquely distinct feature "wherein the Micom is arranged to save the image signal in the memory by outputting a storage start signal with respect to the image signal when the first command signal is input from the comparator, and the Micom is arranged to end storage of the image signal by outputting a storage end signal when the second command signal is input from the comparator".

Conclusion

8. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 10:OOAM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Jean Lesperance

Art Unit 2629

Date10/19/2007

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600